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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,234	12/01/2003	Erik Lilliebjerg	NVID-P000638	3722

7590 05/03/2007

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EXAMINER	
BROWN, MICHAEL J	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
05/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,234	LILLIEBJERG, ERIK	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/21/2006* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Schieve(US Patent 6,018,808).

As to claim 1, Schieve discloses a multi-tasking bootstrap system comprising a bus(host bus 16, see Fig. 1) for communicating information, a non-volatile memory(ROM 20, see Fig. 1) communicatively coupled to the bus, the non-volatile memory for storing boot up information(details of master handler 56, see column 4, lines 52-53) including information associated with an interrupt vector table(see column 3, lines 57-61), and a processor(microprocessor 10, see Fig. 1) communicatively coupled to the non-volatile memory the processor configured to retrieve the boot up information from the non-volatile memory including retrieving the information associated with the interrupt vector table(see column 4, lines 32-34), and perform multi- tasking operations while accessing serial presence detect information(pertinent information relative to that on which microprocessor 10 had been working; see column 4, lines 41-42) during boot up operations prior to completing volatile memory initialization(see column 4, lines 40-44).

As to claim 2 Schieve discloses a multi-tasking bootstrap system wherein the non-volatile memory is a read only memory(see column 3, line 39).

As to claim 3, Schieve discloses a multi-tasking bootstrap system wherein the bus is a system management bus(see column 3, line 38).

As to claim 4, Schieve discloses the multi-tasking bootstrap system wherein communications via the system management bus are controlled by a system management bus controller(bus controller 18, see Fig. 1) operating in an interrupt driven mode.

As to claim 5, Schieve discloses the multi-tasking bootstrap system wherein the system management bus communicates serial presence detect data(pertinent information relative to that on which microprocessor 10 had been working; see column 4, lines 41-42) in accordance with directions from a system management bus controller(bus controller 18, see Fig. 1) operating in an interrupt driven mode.

As to claim 6, Schieve discloses the multi-tasking bootstrap system wherein the serial presence detect data includes memory description information(see column 4, lines 5-10 and 40-44).

As to claim 7, Schieve discloses a multi-tasking bootstrap system wherein the non-volatile memory includes basic input/output system instructions that direct the processor in performing an interrupt driven initialization of a volatile memory and multi-tasking operations between interrupt operations(see column 3, lines 43-61).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schieve(US Patent 6,018,808) further in view of Skrovan et al.(US Patent 6,016,554).

As to claim 8, Schieve discloses a multi-tasking bootstrap method comprising accessing interrupt vector table(see column 3, lines 57-61) information stored in a non volatile memory(ROM 20, see Fig. 1) (see column 4, lines 32-34), initializing a program interrupt controller(PIC)(PIC 32, see Fig. 2), a system management bus controller(bus controller 18, see Fig. 1), and operating the system management bus controller in a multitasking environment in which the system management bus controller operates in an interrupt driven mode prior to completing volatile memory initialization(see column 4, lines 40-44), wherein the operating the system management bus controller includes retrieving serial presence detect data(pertinent information relative to that on which

microprocessor 10 had been working; see column 4, lines 41-42). However, Schieve fails to specifically disclose programming the system management bus controller.

Skrovan teaches a system management bus controller(control signal generator 24, see Fig. 2) that is programmable(see column 7, line 67- column 8, line 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Skrovan's programmable control signal generator 24 with Schieve's multi-tasking bootstrap method in order to adjust bus controller 18. The motivation to do so would be to generate a chosen control signal following detection of a trigger event(see Skrovan column 8, lines 1-3).

As to claim 9, Schieve discloses the multi-tasking bootstrap method wherein the interrupt vector table information is accessed when an interrupt indication is triggered(see column 3, lines 57-61).

As to claim 10, Schieve discloses the multi-tasking bootstrap method wherein the non-volatile memory is a read only memory(ROM)(ROM 20, see Fig. 1).

As to claim 11, Schieve discloses the multi-tasking bootstrap method wherein the interrupt vector table information is accessed at a pre-memory initialization stage when a system is started up(see column 3, lines 11-13).

As to claim 12, Schieve discloses the multi-tasking bootstrap method wherein the interrupt vector table information is accessed before completing random access memory initialization(see column 3, lines 11-13).

As to claim 13, Schieve discloses the multi-tasking bootstrap method wherein the interrupt vector table information is accessed as a processor(microprocessor 10, see

Fig. 1) is performing initial basic input/output system operations (BIOS), including during a power on self test (POST)(POST; see column 3, line 51) (see column 3, lines 11-13).

As to claim 14, Skrovan teaches the multi-tasking bootstrap method wherein the programming of the system management bus controller includes initializing the system management bus controller(see column 7, line 64- column 8, line 3).

As to claim 15, Skrovan teaches the multi-tasking bootstrap method wherein the system management bus programming includes slamming system management bus resource addresses(see column 9, lines 56-59).

As to claim 16, Schieve discloses the multi-tasking bootstrap method wherein multi-tasking operations are executed while processes for retrieving the serial presence detect data are performed(see column 4, lines 40-44).

As to claim 17, Schieve discloses the multi-tasking bootstrap method further comprising providing a location where serial presence detect data is located, retrieving the serial presence detect data in an interrupt driven mode, performing multi-tasking operations while waiting for the serial presence detect data to be retrieved, and generating an interrupt when the serial presence detect data is retrieved(see column 4, lines 31-48).

As to claim 18, Schieve discloses a computer system comprising a display device(device 42, see Fig. 2) coupled to a bus(host bus 16, see Fig. 1), a non-volatile memory unit(ROM 20, see Fig. 1) coupled to the bus, and a processor(microprocessor 10, see Fig. 1) coupled to the bus, the processor for executing a method of multitasking boot up initialization processes(see column 4, lines 40-44). Schieve discloses the

method comprising initializing the processor to access interrupt vector table information stored in the non-volatile memory unit(see column 4, lines 32-34), initializing a program interrupt controller (PIC)(PIC 32, see Fig. 2), a system management bus controller(bus controller 18, see Fig. 1), and operating the system management bus controller in a multitasking environment in which the system management bus controller operates in an interrupt driven mode prior to completing volatile memory initialization(see column 4, lines 40-44), wherein the operating the system management bus controller includes retrieving serial presence detect data(pertinent information relative to that on which microprocessor 10 had been working; see column 4, lines 41-42). However, Schieve fails to specifically disclose programming the system management bus controller.

Skrovan teaches a system management bus controller(control signal generator 24, see Fig. 2) that is programmable(see column 7, line 67- column 8, line 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Skrovan's programmable control signal generator 24 with Schieve's multi-tasking bootstrap method in order to adjust bus controller 18. The motivation to do so would be to generate a chosen control signal following detection of a trigger event(see Skrovan column 8, lines 1-3).

As to claim 19, Schieve discloses the multi-tasking bootstrap creation process further comprising providing a location where serial presence detect is located, retrieving the serial presence detect data in an interrupt driven mode, performing multi-tasking operations while waiting for the serial presence detect data to be retrieved, and

generating an interrupt when the serial presence detect data is retrieved(see column 4, lines 31-48).

As to claim 20, Schieve discloses a multi-tasking bootstrap creation process further comprising temporarily storing serial presence detect data in a processor cache(see column 3, lines 43-55).

Response to Arguments

3. Applicant's arguments, see Remarks, filed 3/27/2007, with respect to the rejection(s) of claim(s) 1-3, and 7 under 35 U.S.C. 102(b) as being anticipated by Schieve(US Patent 6,018,808); claim(s) 8-9, and 11-17 under 35 U.S.C. 102(b) as being anticipated by Skrovan et al.(US Patent 6,016,554); claim(s) 4-6, and 18-20 under 35 U.S.C. 103(a) as being unpatentable over Schieve(US Patent 6,018,808) further in view of Skrovan et al.(US Patent 6,016,554); and claim(s) 4-6 under 35 U.S.C. 103(a) as being unpatentable over Skrovan et al.(US Patent 6,016,554) further in view of Schieve(US Patent 6,018,808) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made for claims 1-7 in view of Schieve(US Patent 6,018,808), and claims 8-20 in view of Schieve(US Patent 6,018,808) and Skrovan et al.(US Patent 6,016,554).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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SUPERVISORY PATENT EXAMINER
4/30/07